WHAT IS CLAIMED IS:

1. A trace control circuit comprising:

determination means for determining whether a CPU outputs a branching source address or a branching destination address, based on a control signal output from the CPU;

address capturing means for capturing the branching source address in an absolute address representation from the CPU, when the determination means determines that the CPU has output the branching source address, and for capturing the branching destination address in a relative address representation, when the determination means determines that the CPU has output the branching destination address; and

outputting means for outputting the branching source address and the branching destination address captured by the address capturing means to a trace bus.

2. The trace control circuit according to claim 1, wherein the determination means demands requests the address capturing means to capture the branching destination address in an absolute address representation, when the control signal output from the CPU indicates an output of the branching destination address in an absolute address representation.

3. A trace control circuit comprising:

address capturing means for capturing a relative address in a memory accessed by a CPU;

data capturing means for capturing access data of the CPU; and

output means for outputting a reference address to a trace bus and outputting the relative address in the memory captured by the address capturing means and the access data captured by the data capturing means.

4. The trace control circuit according to claim 3, further comprising:

determining means for determining whether the CPU outputs the relative address in the memory or the absolute address thereof, and for requesting the address capturing means to capture one of the relative address and the absolute address.

5. A trace control circuit comprising:

address capturing means for capturing an address in a memory accessed by a CPU;

data capturing means for capturing data for block transfer; and

output means for outputting to a trace bus the address captured by the address capturing means and the data captured by the data capturing means upon a first access in the block transfer, and for outputting the data captured by the data

capturing means to the trace bus upon a second and subsequent accesses.

6. The trace control circuit according to claim 5, wherein the output means outputs a reference address to the trace bus, when the address captured by the address capturing means is a relative address.